REMARKS

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 7, 11, 12-14 and 19

Claims 1, 7, 11, 12-14 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,006,511 issued to Lanzafame et al. (*Lanzafame*) in view of U.S. Patent No. 5,812,860 issued to Horden (*Horden*), further in view of U.S. Patent Application Publication No. 2003/0115428 issued to Zaccarin (*Zaccarin*). Applicant submits these claims are not obvious in view of *Lanzafame, Horden* and *Zaccarin* for at least the reasons set forth below.

Claim 1 recites, in part, the following:

> monitoring a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware components include at least a processor **that performs simultaneous multi-threading** and a buffer;
>
> coordinating dispatch of a plurality of threads in the system at least in part **to increase execution overlap of the threads**, wherein at least one of the threads is associated with the application;

Independent claim 14 recites similar limitations. The Office action correctly concedes that *Lanzafame* fails to disclose coordinating dispatch of one or more threads in the system at least in part to increase execution overlap and dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads. *Lanzafame* also admittedly fails to disclose a processor as one of the configurable hardware components. Accordingly, *Lanzafame* necessarily fails to disclose a processor that performs simultaneous multi-threading.

Horden is cited as curing the deficiencies of *Lanzafame*. However, *Horden* also fails to disclose a processor that performs simultaneous multi-threading. Without

simultaneous multi-threading capabilities in the processor, Applicant is unaware of how multiple threads could execute simultaneously (i.e., overlapping execution), as claimed. Indeed, while the Office action concedes that *Lanzafame* fails to disclose coordinating dispatch of one or more threads at least in part in increase execution overlap, the Office action does not even suggest that *Horden* discloses coordinating dispatch of threads to increase execution overlap.

As claimed, when dispatch of threads is coordinated to increase execution overlap and the frequency and/or voltage of the processor is dynamically adjusted based on the state of the application and the state of the threads (e.g., frequency and/or voltage might be adjusted higher when threads are executing and adjusted lower when threads are not executing), power consumption is reduced. While *Horden* allegedly discloses techniques for reducing power consumption, *Horden* does not disclose the techniques claimed herein for reducing power consumption in a processor that performs simultaneously multi-threading. Thus, Applicant submits the combination of *Lanzafame* and *Horden* fails to disclose at least one limitation of the independent claims 1 and 14. Accordingly, Applicant submits claims 1 and 14 are not obvious in view of *Lanzafame* and *Horden*.

Claims 7, 11, 12-13 and 19 depend from claims 1 and 14, respectively. Given that dependent claims necessarily include the claims from which they depend, Applicant submits claims 7, 11, 12-13 and 19 are not obvious for at least the same reasons claims 1 and 14 are not obvious.

Claims 2-4 and 15

Claims 2-4, 10 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lanzafame, Horden* and *Zaccarin* further in view of various other cited references: specifically, claims 2-4 and 15 in view of U.S Patent No. 6,662,203 issued to Kling et al. (*Kling*); and claim 10 in view of U.S Patent Application Publication No. 2002/018884 issued to Jain et al. (*Jain*). Applicant submits these claims are not obvious in view of the cited references for at least the reasons set forth below.

Claims 2-4, 10 and 15 depend from claims 1 and 14, respectively. As discussed above, claims 1 and 14 are not obvious in view of *Lanzafame* and *Horden* for at least the reasons that the cited references fail to disclose coordinating dispatch of threads to increase execution overlap, where the threads are executed by a processor capable of simultaneous multi-threading. *Kling* is cited as disclosing a thread having one or more activities and assessing execution readiness of the one or more activities. *Jain* is cited as disclosing increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system. Whether or not these references disclose the limitations cited in the Office action, neither *Kling* nor *Jain* disclose coordinating dispatch of threads to increase execution overlap, where the threads are executed by a processor capable of simultaneous multi-threading, as claimed. Thus, *Kling* and *Jain* fail to cure the deficiencies of *Lanzafame* and *Horden*. Accordingly, Applicant submits claims 2-14, 10 and 15 are not obvious in view of the respective cited prior art.

Claims 39-41 and 44-50

Claims 39-41 and 44-47 and 48-50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Zaccarin* in view various other cited references: specifically, claims 39 and 41 in view of *Lanzafame* and further in view of *Horden*; claim 40 in view of *Lanzafame*, *Horden* and further in view of *Kling*; claims 44-47 in view of *Kling* further in view of U.S. Patent No. 5,668,993 issued to Peter et al (*Peter*); and claims 48-50 in view of *Kling*. Applicant notes that the examination of the claimed invention and the application of these numerous references is a significant task; Applicant thanks the Examiner for the thorough examination and the thorough analysis of the references.

Applicant respectfully submits that these claims are not rendered obvious by the cited references for at least the following reasons. Each of the rejections made above is based on the application of *Zaccarin*, which is defective given that *Zaccarin* fails at least to disclose a multi-threaded processor, as claimed in each of the independent claims. The other cited references do not cure the deficiencies noted above in that they also fail at least to disclose a multi-threaded processor. Applicants respectfully submit that a prima facie case of obviousness under MPEP § 2143 has not been established with respect to the independent claims, at least for failing to establish that the cited references disclose every element of the claimed invention. Because the independent claims are nonobvious, the dependent claims are also nonobvious.

CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections have been overcome. Therefore, claims 1-4, 7, 10-15, 19, 39-41 and 44-50 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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